REMARKS

Applicant requests reconsideration and withdrawal of the rejections set forth in the above-mentioned Office Action, in view of the foregoing amendments and the following remarks.

Claims 1 and 3-18 remain pending in this application, with Claim 1 being the sole independent claim. By this Amendment, Applicant has amended Claims 1 and 15.

Claims 1, 3-6, and 8-18 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application Publication No. 2004/0042705 A1 (Uchida, et al.), in view of statements made in Applicant's own application concerning conventional systems. Claim 7 stands rejected under 35 U.S.C. § 103 as being unpatentable over Uchida, et al. and Applicant's own application, in view of U.S. Patent No. 4,845,702 (Melindo). Applicant traverses these rejections.

As recited in independent Claim 1, Applicant's invention is directed to an optical waveguide device. The device includes a slab-type optical waveguide layer and a plurality of chips which include optical input and output ports for inputting and outputting an optical signal. An optical input port receives an optical signal, output by an optical output port, from the slab-type optical waveguide layer in accordance with a timing control signal inputted using an electrical connection between the plurality of chips. The timing control signal is an electrical signal obtained by dividing a clock frequency for the optical signal.

The Office Action cites Uchida, et al. as teaching all of the features of the present invention except for the slab-type optical waveguide, which the Office Action argues

would be obvious from the discussion of an optical fiber in Uchida, et al. The Office Action does not discuss how Uchida, et al. applies to the timing control signal discussed in independent Claim 1. Further, independent Claim 1 now recites that the timing control signal is an electrical signal obtained by dividing a clock frequency for the optical signal. Applicant submits that Uchida, et al. does not describe or suggest such a timing control signal.

Melindo is cited in the Office Action as describing the use of a packet signal train formed of a finite pulse train for time division packet switching. Regardless of whether Melindo sufficiently describes the packet signal train of the present invention, Applicant submits that that patent does not describe or suggest the timing control signal discussed above with respet to Uchida, et al.

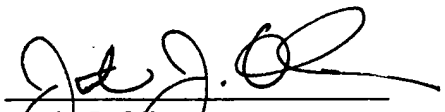
Accordingly, Applicant submits that Uchida, et al. and Melindo, taken alone or in combination, fail to disclose or suggest at least the features of an optical input port receiving an optical signal, output by an optical output port, from the optical waveguide layer in accordance with a timing control signal using an electrical connection between the plurality of chips, wherein the timing control signal is an electrical signal obtained by dividing a clock frequency for the optical signal, as recited in independent Claim 1.

Applicant submits that the dependent claims are allowable, in their own right, for defining features of the present invention in addition to those recited above with respect to independent Claim 1. Applicant requests individual consideration of the dependent claims.

For the foregoing reasons, Applicant requests withdrawal of the rejections under 35 U.S.C. § 103.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our address given below.

Respectfully submitted,



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